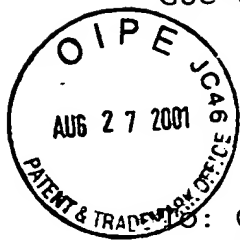GUC-00-002

August 27, 2001

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
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Subject:

Serial No. 09/887,783 06/25/01

Chuang Cheng, Chih-Tsun Huang,
Jing-Reng Huang, Cheng-Wen Wu

TEST PATTERN GENERATOR FOR SRAM
AND DRAM

Grp. Art Unit: 2133

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation

In An Application.

The following Patents and/or Publications are submitted to

comply with the duty of disclosure under CFR 1.97-1.99 and

37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,377,148 to Rajsuman, "Apparatus and Method

to Test Random Access Memories for a Plurality of Possible

Types of Faults", describes hardware and methods to test

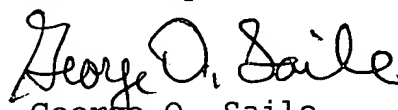variable size RAMs in a constant period of time.

U.S. Patent 5,764,657 to Jones, "Method and Apparatus for Generating an Optimal Test Pattern for Sequence Detection", presents a method for generating an optimal serial test pattern for sequence detection.

U.S. Patent 6,061,817 to Jones et al., "Method and Apparatus for Generating Test Pattern for Sequence Detection", presents a method and apparatus for generating a serial test pattern for sequence detection.

U.S. Patent 6,094,738 to Yamada et al., "Test Pattern Generation Apparatus and Method for SDRAM", presents a test pattern generation apparatus and method for an SDRAM by adding a wrap address conversion circuit.

Kim et al., "On Comparing Functional Fault Coverage and Defect Coverage for Memory Testing," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 18, No.11, November 1999, IEEE pp. 1676-1683, describes the evaluation of the effectiveness of the memory testing algorithms based on the defect coverage by comparing the defect coverage of known memory testing algorithms using the same defect statistics.

Sincerely,

George O. Saile,
Reg. No. 19572